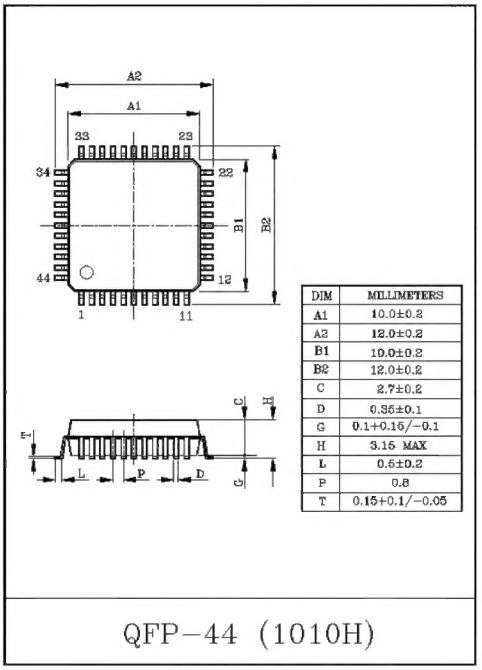
ADVANCED FM PROCESSOR

KIA2093F is an advanced FM processor for car tuners. Integrating IF, PNR and stereo decoder on a single chip, KIA2093F is designed to improve performance while drastically reducing external parts and adjustment steps. Car tuners with both FM/AM require only the KIA2074F prior-stage super RF processor and KIA2093F, delivering excellent cost efficiency.



DIM	MILLIMETERS
A1	10.0±0.2
A2	12.0±0.2
B1	10.0±0.2
B2	12.0±0.2
C	2.7±0.2
D	0.35±0.1
G	0.1+0.15/−0.1
H	3.15 MAX
L	0.5±0.2
P	0.8
T	0.15+0.1/−0.05

QFP-44 (1010H)

FUNCTIONS

IF Block
- IF Limiter amp with passband set
- Quadrature FM detection
- High-speed field strength detection using internal main slider
- Field strength detection using bottom peak detector
- Field strength detection muting
- Detuning muting using field strength detection muting
- Station detection with speed-up
- IF count output by request

PNR Block
- Signal delay
- Signal retection
- FM pulse noise detection
- AM pulse noise detection
- Over-deviation protector (ODP)
- Operating supply voltage : V_{CC}=7~9V

Stereo Decoder Block
- Adjustment-free 912kHz PLL
- Adjustment-free pilot cancel
- Full-separation trimmer
- Blend control using internal custom-made slider
- High-cut control using internal custom-made slider
- 114kHz anti-birdie stereo decoder

FEATURES

Block Overviews

- Exceptional cost performance compared to current FM processor (KIA6072AF)

Adjustment points	: 5	→2	(60% reduction)
Printed circuit board	: Double sided	→Single-sided	(⅓～¼ cost reduction)
Number of electrolytic capacitors	: 6	→3	(About 50% reduction)
Number of external parts	: Around 100	→55	(About 45% reduction)

IF Block

- High-performance IF limiter amp with passband set and high-performance quadrature FM detector provide excellent limiter sensitivity and AM rejection (AMR).
  Because the limiter sensitivity is so high, and external IF amp between the two processors is not required.
  When Vi(lim.)≃16dBμV(Typ.) 1kHz, ±75kHz Dev.
  When AMR≧50dB (Typ.) Vi≃50～118dBμV
  When AMR=70dB (Typ.) Vi≃70～110dBμV
- The temperature coefficient of the IF limiter amp is the inverse of that of the RF processor, eliminating the conventional need for a thermistor for an external IF amp.
- At application, obtains superior characteristics against tweet interference in the weak-to-strong field strength range.
  $\Delta N \leqq +1dB$(Typ.) at f_R=96.3MHz/107MHz
  ⊿N=change in N at 98.1MHz
- Remarkably low fo temperature deviation and station detection band width temperature deviation.
  $\Delta fo \leqq \pm 15kHz$ (Typ.)
  $\Delta B_W(SD) \simeq 0kHz$(Typ.) when $B_W(SD)$=135kHz, Ta=-40～85℃
- A convenient, variable main slider is built in to set optimal field strength detection muting and station detection based on field strength detector output. Also, to obtain optimal blend control and high-cut control without deviation caused by external parts.
  These functions can be set by a circuit with a single variable resistor for the slider amount setting, thus reducing the number of adjustment steps.
- A convenient bottom peak detector output is provided to detect rapid changes in field strength obtained from the slider output, and to detect multipath interference. The bottom peak detector output can be used for controlling blend and high-cut.
- The field strength detection muting sensitivity and the attenuation can be set as desired. The detuning muting attenuation is roughly proportional to the field strength detection muting.
- The station detector sensitivity and the bandwidth can be set as desired.
  The sensitivity and bandwidth for the detuning muting bandwidth change to about the same degree as station detection.
  Moreover, an on-request speed-up can be achieved without additional parts.
- The IF count output can be set on/off by an external request.

PNR Block

- Pulse noise reduction achieves a 10dB-improvement over conventional noise reduction by using a stable delay at the signal delay circuit and by the effective detection bandwidth of the noise pass filter.
- With AM pulse noise detection, the pulse noise reduction at weak field strength is equivalent to the pulse noise reduction at medium field strength.
- An over-deviation protector forcibly stops the operation of the trigger pulse at over-deviation and prevents transition distortion caused by PNR malfunction.

Stereo decoder block

- Because the adjustment-free PLL is used, VCO free-run frequency adjustment is not necessary. The use of a 912kHz resonator can contribute to a low physical profile.
- As the adjustment-free pilot canceler is a cancel loop independent of the pilot detector, cancellation is improved by 10dB over conventional cancellation. Pilot cancellation≃30dB (Typ.)
- As a full-separation trimmer function is built in, high separation is achieved regardless of what IF-stage external ceramic filters are combined.

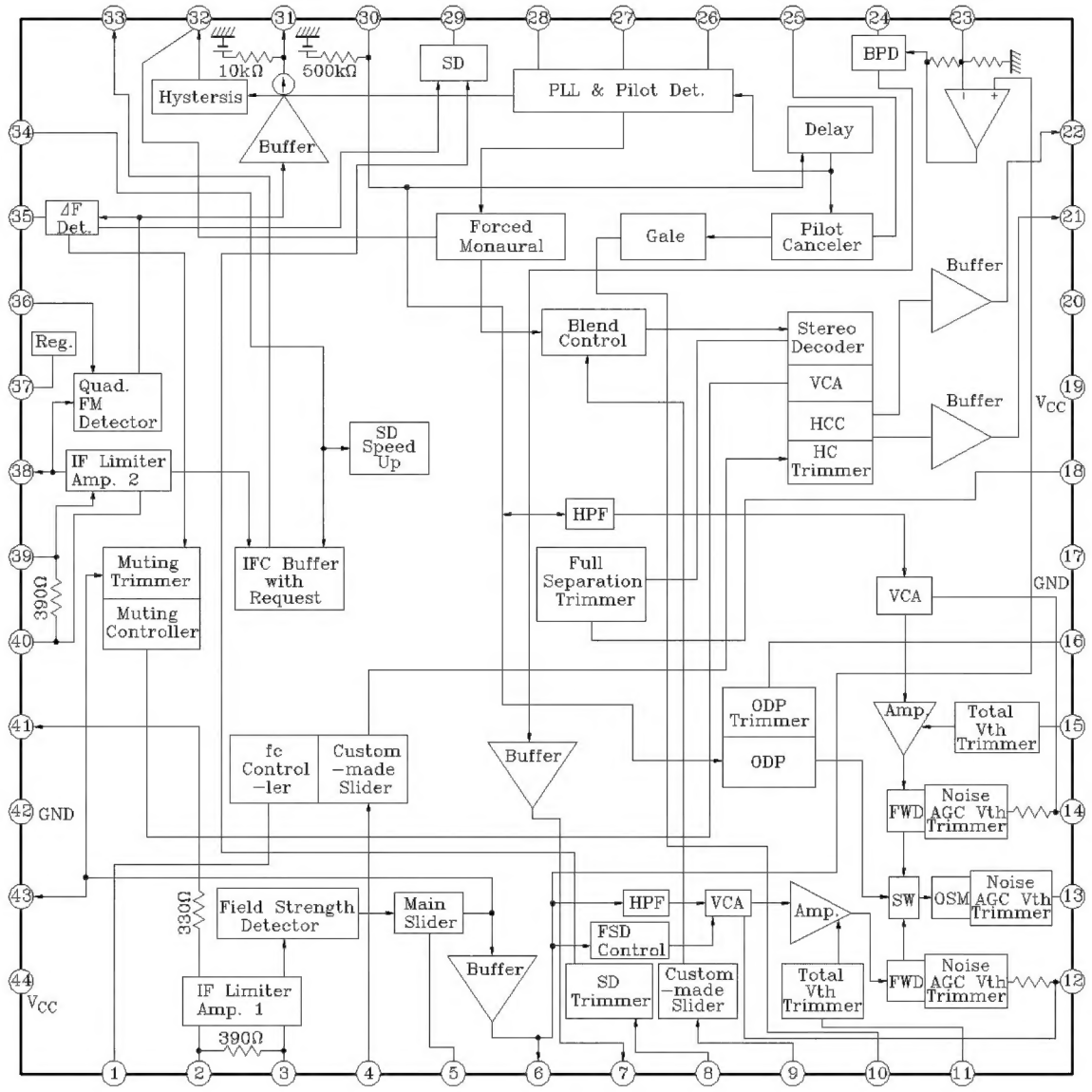
Example : sep.≃40dB(Typ.) when BW=180kHz, three IF filters used, 100~10kHz±75kHz Dev.

- Because the blend control pin and the high-cut control pin can be controlled by a high-impedance signal source, the processor allows the omission of an electrolytic capacitor for the time constant even if the pins are directly controlled from the field strength detector output. When controlling using the bottom peak detector output, neither side requires a capacitor.
- As a custom-made slider is built into both input pins, an LED or diode is no longer required.
- Also, high-cut control no longer requires a high-cut capacitor but can be set using just on external resistor.
- Because a cutoff-frequency-reduction-type high-cut is used after left and right separation, quieting noise at a weak field can be effectively reduced with no interference to the blend control.
- A 114kHz anti-birdie stereo decoder prevents birdie noise interference and improves interference resistance within the FTZ band.

PIN NAME

PIN NO.	PIN SYMBOL	PIN NAME	PIN NO.	PIN SYMBOL	PIN NAME
1	HCT	High-cut trimmer	23	Noise-Amp in	Noise amp input
2	IFA1 Bias	IF amp 1 bias	24	BPD	Bottom peak detector
3	$IFA1_{in}$	IF amp 1 input	25	PC	Pilot cancel
4	HCC	High-cut control	26	PD1	Phase detector
5	Slide Trimmer	Slide trimmer	27	VCO	VCO
6	FSD	Field strenah detector	28	PD2	Pilot detector
7	BPDout	Bottom peak detector output	29	SD	Station detector output
8	SDS Trimmer	Station detector sensitivity trimmer	30	PNRin	Pulse noise reduction input
9	BC	Blend control	31	Compo.	FM detector output
10	Hold	Hold	32	Mode-out	Stereo mode output
11	PNS Trimmer	FSD-system pulse noise detection sensitivity trimmer	33	IFC	IF count output
12	NAGC Trimmer	FSD-system noise AGC detection sensitivity trimmer	34	Request	Request pin
13	TPW Trimmer	Trigger pulse width trimmer	35	⊿F	⊿F detector
14	NAGC Trimmer	FM detector-system noise AGC dectection sensivity trimmer	36	Quad.	Quadrature detector
15	PNS Trimmer	FM detector-system pulse noise detection sensivity trimmer	37	Reg.	Requlator
16	ODP Trimmer	Over-deviation trimmer	38	IFA2out	IF amp 2 output
17	GND	Ground	39	IFA2in	IF amp 2 input
18	Sep.	Separation trimmer	40	IFA2 Bias	IF amp 2 bias
19	V_{CC}	Power supply	41	IF1out	IF amp 1 output
20	Bias	Bias	42	GND	Ground
21	L	L-channel output	43	Muting	Muting
22	R	R-channel output	44	V_{CC}	Power supply

BLOCK DIAGRAM

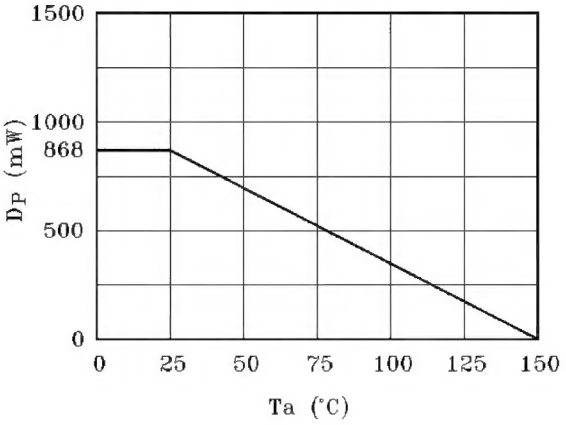


MAXIMUM RAGINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	10	V
Power Dissipation	P_D (Note)	868 (IC only)	mW
Operating Temperature	T_{opr}	-40~85	℃
Storage Temperature	T_{stg}	-55~150	℃

Note : When operating at temperatures higher than 25℃, maximum power dissipation decreases by 6.94mW for every 1℃ over 25℃. See Fig.1 for the relationship between power dissipation and ambient temperature during operation.

POWER DISSIPATION (P_D)- AMBIENT TEMPERATURE (Ta)



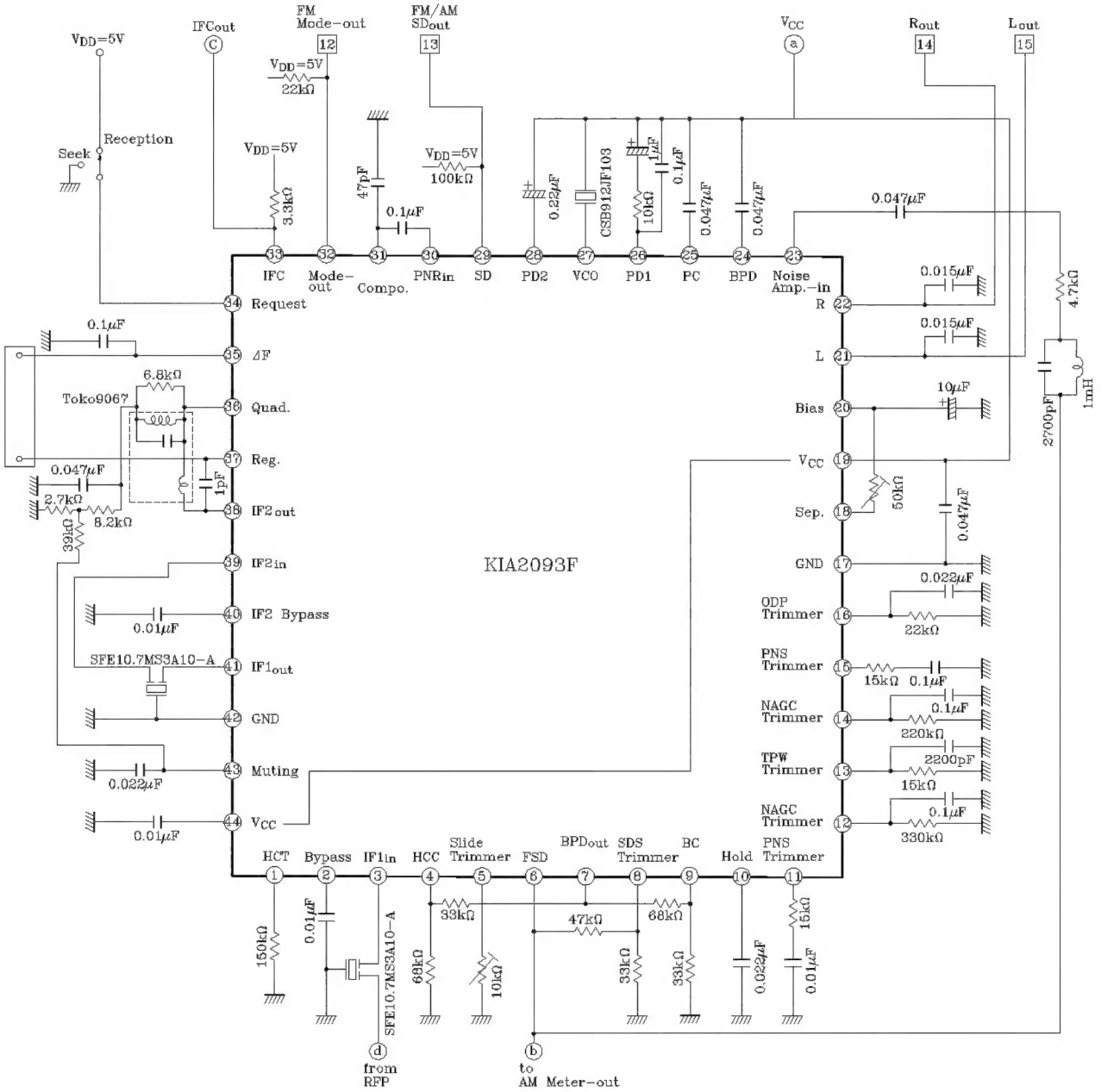
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Vcc=8.5V, fi/Vi=10.7MHz/100dBμV, fm/Dev.=mono 400Hz/75Hz, Vi(Req)=5V, stereo decoder output monitor, Ta=25℃)

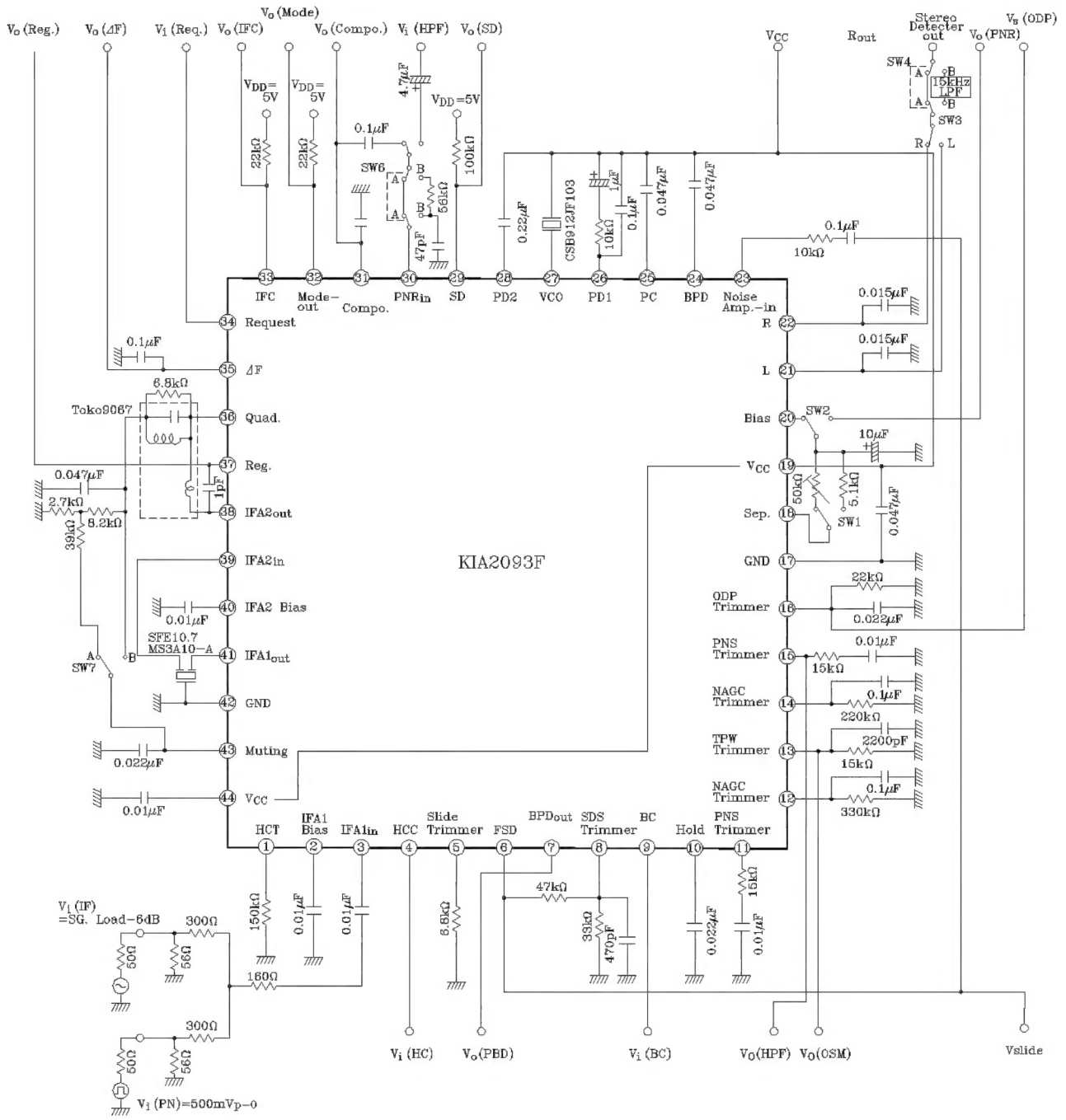
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
FM Mode Supply Current	I_{CC1}	-	Vi=-20dBμV, SW_7=A	45	55	68	mA
	I_{CC2}	-	Vi=-100dBμV, SW_7=A	-	60	-	
Decoder Output	V_O	-	0dB=440mVrms	-2	0	2	dB
Decoder Output L,R Deviation	ΔV_O	-	SW_3=L→R	-1	0	1	dB
AM Rejection Ratio	AMR	-	Dev.=0kHz, AM 1kHz, 30%	-	70	-	dB
Slider Output	Vslide 0	-	Vi=-20dBμV, Dev.=0kHz	-	0.1	-	V
	Vslide 1		Vi=-50dBμV, Dev.=0kHz	0.3	1.0	1.7	
	Vslide 2		Vi=-80dBμV, Dev.=0kHz	-	4.0	-	
	Vslide 3		Vi=-100dBμV, Dev.=0kHz	5.1	6.0	6.7	
	Vslide 4		Vi=-110dBμV, Dev.=0kHz	-	6.5	-	
Multipath Detection Sensitivity	$V_{S(Multi)}$	-	19kHz AM=0→rising When V_O(BPD)=-5%	-	60	-	%
Limiting Sensitivity	$V_{i(lim.)1.}$	-	V_i variable Point Where V_O-3dB	-	16	-	dBμV
Soft Muting Sensitivity	$V_{i(lim.)2.}$	-	V_i variable Point Where V_O-3dB SW_7=A	46	54	62	dBμV
Amount of Soft Muting	ATT(soft)	-	V_i=-20dBμV, SW_7=B→A	-	24	-	dB
Amount of Detuning Muting	ATT (Detune)	-	fi=10.7MHz →10.8MHz, fi=10.7MHz →10.6MHz, SW_7=A	-	29	-	
Station Detection Bandwidth							
Station Detector Sensitivity	$BW_{(SD)}$	-	$V_{O(SD)}$=≃0→5V, Dev.=0kHz, $V_{i(IF)}$ variable, SW_3=L	105	135	165	kHz
	$V_{S(SD)}$			58	64	70	dBμV
Request Sensitivity	$V_{S(req)}$	-	Vi(req.)=Variable, Dev.=0kHz	1.8	2.3	2.8	V
Mono Distortion Ratio	THD(mono)	-	Dev.=22.5kHz	-	-55	-	dB
Stereo Distortion Ratio	THD(stereo)	-	L+R/P=27%/10%	-	-56	-50	
	THD(Sub)	-	L-R/P=27%/10%	-	-55	-	
IF Count Output	V_O(IFC)	-	Vi(req.)=5V, Dev.=0kHz	104	109	115	dBμV

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Stereo Separation	Sep.(1kHz)	-	fm=1kHz Lonly or Ronly/P=90%/10% SW_2=L→R and R→L		40	45	-	dB
Mono S/N Ratio	S/N (mono)	-	Dev.=75kHz→0kHz		-	70	-	
Stereo S/N Ratio	S/N (stereo1)	-	L+R/P=90%/10%→0%/10%		63	70	-	
Signal/Residual Carrier Ratio	S/N (stereo2)	-	SW_4=-B→A L+R/P=90%/10%→0%/10%		37	49	-	
HPF Cutoff Frequency	fc(HPF)	-	Vo(HPF)-3dB point V_i(IF), V_i(HPF) input	Det.	-	140	-	kHz
				FSD	-	75	-	
Signal/Residual Pulse Ratio	S/N(PNR)	-	fm/Dev.=400Hz/75kHz V_i(PN)=500mV_{P-0} tW=10μS, fi=1kHz		61	66	-	dB
Deviation Detection Sensitivity	Vs(Dev.)	-	V_i(IF), V_i(PN) input f/tw=1kHz/10μS, Dev. deviation variable Point where Vo(OSM)=0V		-	90	-	kHz
Gate Release Time	tG	-	V_i(IF), V_i(PN) input tW=10μS, f_i=1kHz Vo(PNR) monitor		-	53	-	μS
High-Cut Control Attenuation	ATT(HC1)	-	V_i(HC)=2.5V→1.9V	fm=10kHz	0.0	0.2	1.0	dB
	ATT(HC2)	-	V_i(HC)=2.5V→1.1V		6	7	8	
High Cutoff Frequency	fc(HC)	-	V_i(HC)=0V, V_i(HPF) input		-	4.3	-	kHz
Blend Control Attenuation	ATT(BC1)	-	V_i(BC)=2.5V→1.7V	L-R/P= 90%/10%	0	0.2	1.5	dB
	ATT(BC2)	-	V_i(BC)=2.5V→0.9V		23	32	-	
Pilot Sensitivity	$V_{S(PILOT)}$	-	fm/Dev.=19Hz/variable		1.6	2.4	3.2	kHz
Pilot Sensitivity Hysteresis	Hys	-	Vo(Mode) monitor		-	4	-	dB
19kHz PLL Capture Range L	CR (L)	-	fm/Dev.=Variable/7.5kHz		-	1.9	-	%
19kHz PLL Capture Range H	CR (H)	-	fm/Dev.=Variable/7.5kHz		-	2.4	-	%

APPLICATION CIRCUIT....Japanese specifications (RF processor block)

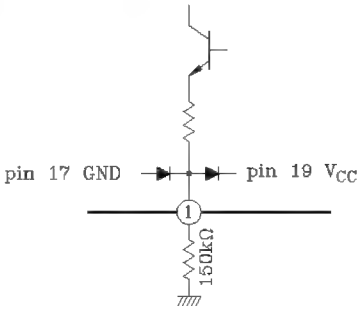
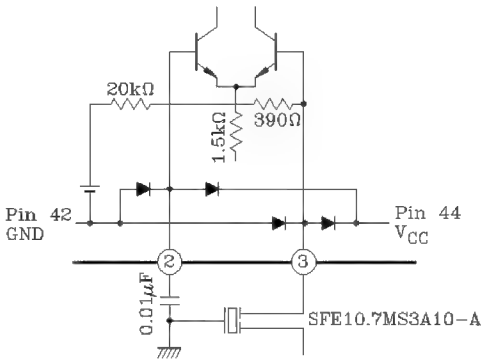


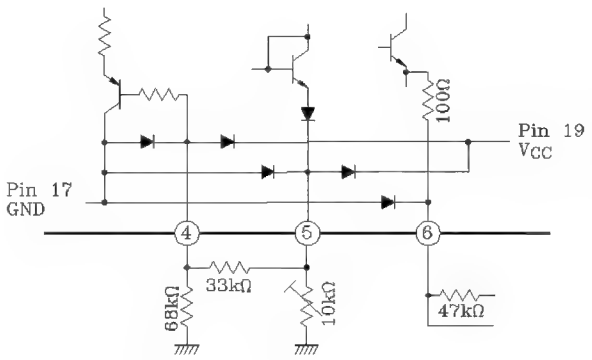
TEST CIRCUIT

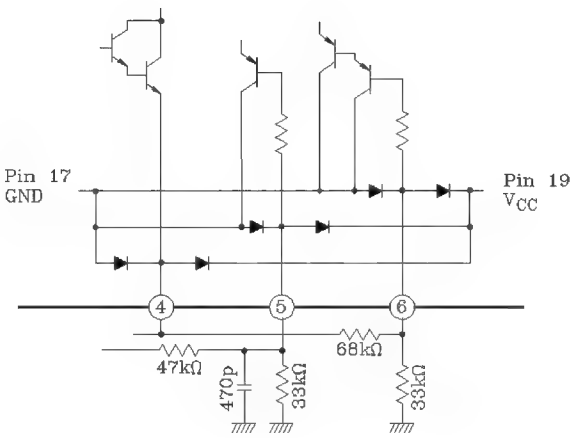


DESCRIPTION OF PIN FUNCTIONS

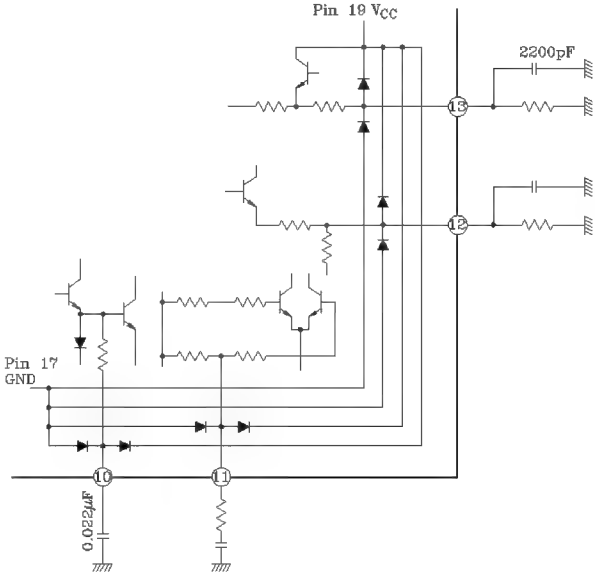
(Pin voltage are typ. values when V_{CC}=8.5V, Ta=25℃, test circuit, no AC input signal)

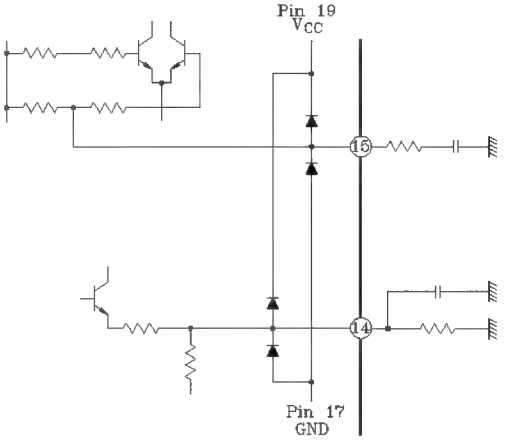
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
1	HCT	1.5		Sets high-cut control cutoff frequency. Set the cutoff frequency using the absolute value of the grounded external resistor. The lower the resistance, the higher the cutoff frequency. The higher the resistance, the lower the cutoff frequency. To release the high-cut, directly ground this pin.
2	IFA1 Bias	2.2		IF limiter amp 1 bias pin. Ground this pin via capacitor.
3	IFA1in	2.2		IF limiter amp 1 input pin. Externally connect a ceramic filter. Incorporates a resistor to allow matching to a 330Ω ceramic filter.

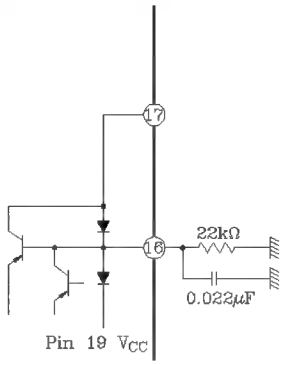
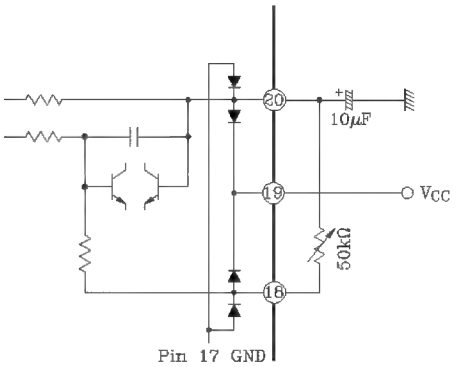
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
4	HCC	0		High-cut control pin. Driven by the voltage obtained by dividing the bottom peak detector output with resistance. Incorporates a high-cut control slider. The amount of high-cut peaks when this pin is around 0.8V.
5	Slide Trim mer	0.5		Sets pin 6 (FSD output) to its optimal value. When the external variable resistor is set to 0Ω,. the amount of slide is approximately equal to 0. The higher the variable resistance, the larger the slide amount.
6	FSD	0		Output the optimum signal meter signal as a voltage. Used for the bottom peak detector, soft muting, and SD. Adjust using the external variable resistor connected to pin 5 (Slide trimmer) so that the optimum value of around 2V is obtained when using an RF processor with Gp=50dB (Eg:KIA2074F) and with 10dBμV on the front-end antenna terminal.

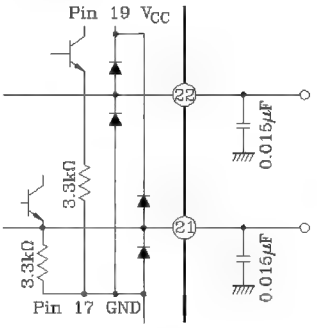
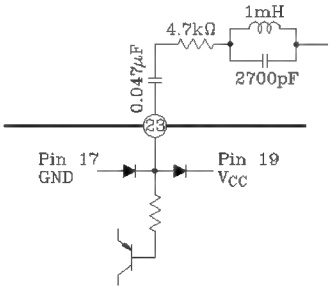
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
7	BPDout	0		Outputs bottom peak detector voltage. Controls pin 9 (Blend control) or pin 4 (High-cut control).
8	SDS Trimmer	0		Sets station detector sensitivity. Externally connect resistors and the capacitor. Set sensitivity by dividing the slide output DC voltage using resistance. The threshold is 1V. The value of the external resistors can be fixed, as meter output from pin 5 (Slide trimmer) is optimal.
9	BC	0		Blend control pin. Driven by the voltage obtained by dividing the bottom peak detector output with resistance. Incorporates a blend control slider. Output is completely mono when this pin is around 0.8V.

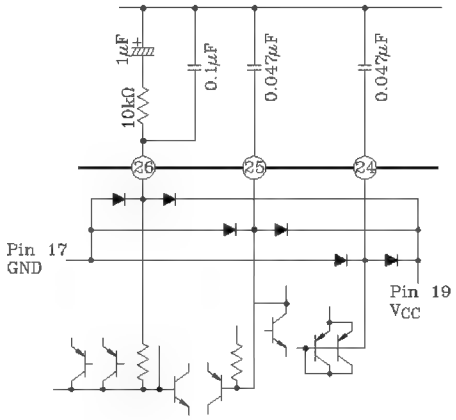
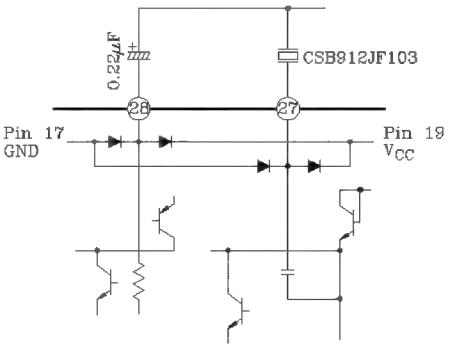
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
10	Hold	1.4		Composite signal hold pin of the FM pulse noise reduction block. Externally connect a 0.022μF capacitor.
11	PNS Trimmer	2.8		Setes the noise AGC operating sensitivity and pulse noise detection sensitivity of the FSD-system FM pulse noise reduction block. Externally connect a capacitor and resistor. The lower the resistance the higher the sensitivity. After setting the sensitivity using this pin, set the noise AGC using pin 12.
12	NAGC Trimmer	0		Sets the noise AGC operating sensitivity of the FSD-system FM pulse noise reduction block. Externally connect a capacitor and resistor. The capacitor should have a low temperature coefficient. Because the higher the resistance the higher the operating sensitivity, the noise AGC is activated by white noise with a stronger field. Even if the pulse noise repetition time shortens, the level of the noise AGC increases.
13	TPW Trimmer	0		Sets the trigger pulse width of the FM pulse noise reduction block. Externally connect a 2200pF capacitor and a resistor. The higher the resistance the wider the trigger pulse.

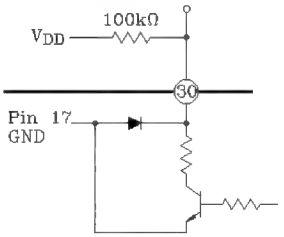
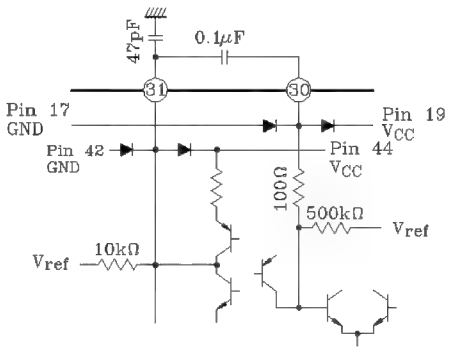
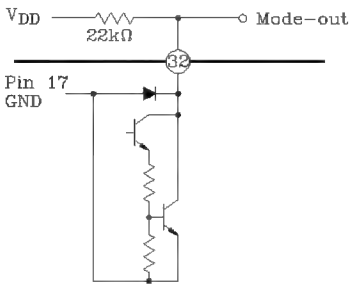


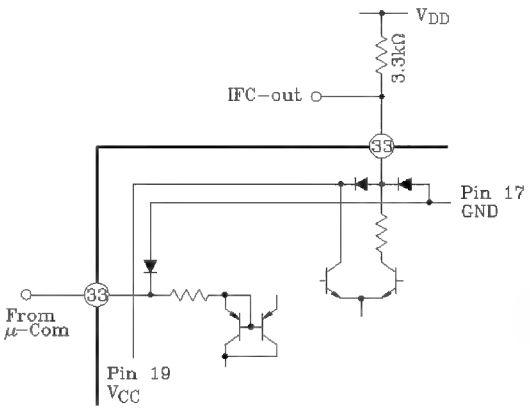
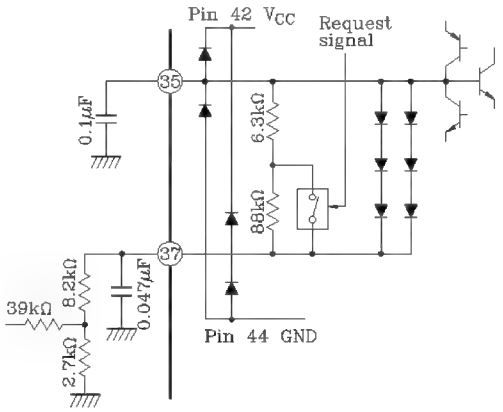
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
14	NAGC Trimmer	0		Sets the noise AGC operating sensitivity of the FM detector-system FM pulse noise reduction block. Externally connect a capacitor and resistor. The capacitance should have a low temperature coefficient. Since the higher the resistance the higher the operating sensitivity, the noise AGC is activated by white noise with a stronger field. Even if the pulse noise repetition time shortens, the noise AGC level increases.
15	PNS Trimmer	2.8		Sets the noise AGC operating sensitivity and pulse noise detection sensitivity of the FM detector-system FM pulse noise reduction block. Externally connect a capacitor and resistor. The lower the resistance the higher the operating sensitivity. After setting the sensitivity using this pin, set pin 14 (Noise AGC).

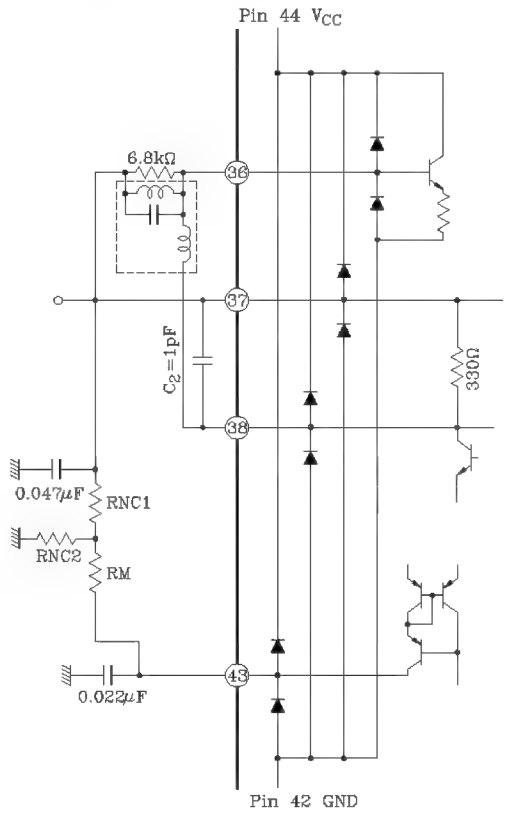
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
16	ODP Trimmer	0		Sets the over-deviation protector (ODP). Externally connect a capacitor and resistor. Indicates the output in accordance with the amount of FM deviation. This output is used to forcibly stop OSM operation of the PNR block, thus preventing PNR malfunction caused by over-deviation. The higher the external resistance the higher the ODP detection sensitivity.
17	GND	0		-
18	Sep.	2.9		Adjusts the full separation of the FM stereo decoder block. Connect an external variable resistor between pins 18 and 20.
19	Vcc	8.5		-
20	Bias	2.9		Stereo decoder reference ground pin for the FM stereo decoder block. Externally connect a capacitor between this pin and GND. Note that low capacitance reduces the low-frequency full separation.

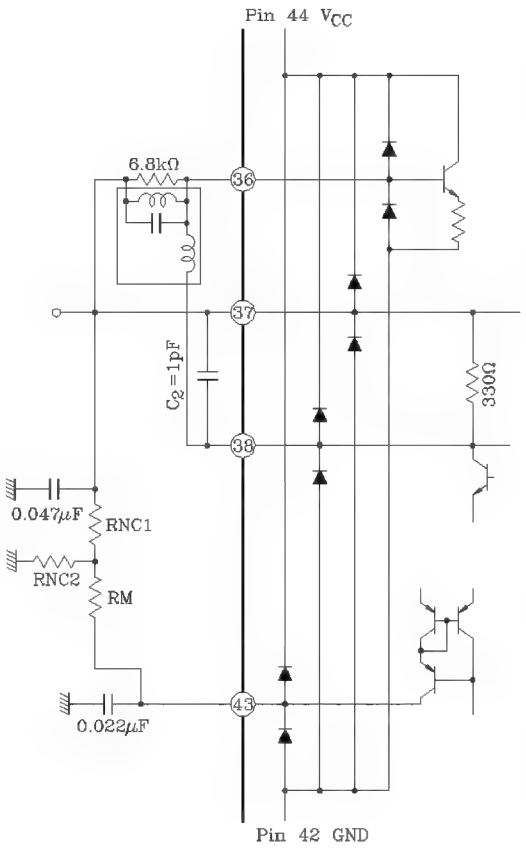
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
21	L	3.2		FM stereo decoder left channel output pin. Externally connect a de-emphasis capacitor.
22	R	3.2		FM stereo decoder right channel output pin. Externally connect a de-emphasis capacitor.
23	Noise-Amp in	0		Subtracts from the DC component of the FSD output (pin6) the AM component and the DC component corresponding to the AM component. Using a parallel resonance circuit consisting of an external capacitor and RL between pins6 and 23, extracts the target frequency component. Prevents malfunction due to the composite signal component. When the DC component of the FSD output is subtracted, almost nothing is subtracted apart from the resonance frequency. Subtraction is performed with about 0dB of gain in the resonance frequency.

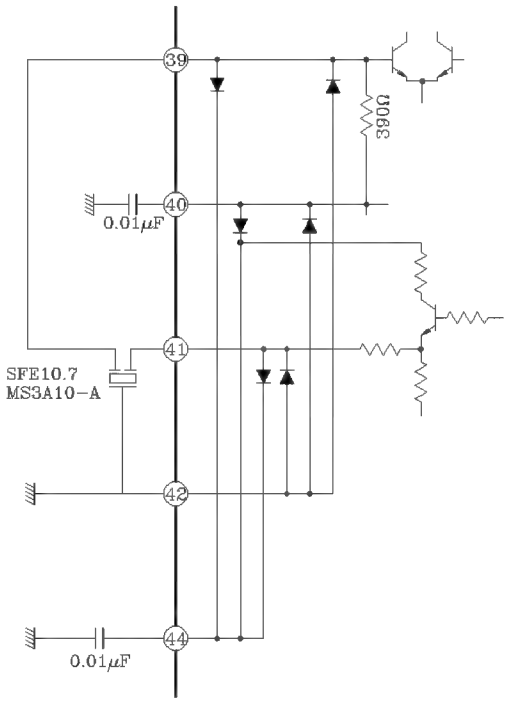
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
24	BPD	0		Bottom peak detector pin connect a capacitor between V_{CC} and this pin. The capacitor is for peak detection. The higher the capacitance the longer the hold time. (The attack time also becomes slightly longer.)
25	PC	7		Pilot cancel control signal generating pin for the FM stereo decoder block. Externally connect a 0.047μF capacitor between this pin and V_{CC}.
26	PD1	6.4		Detects and outputs the PLL phase of the FM stereo decoder block. Externally connect 0.1μF and 1μF capacitors, and a 10kΩ resistor between this pin and V_{CC}. The capacitors should have a low temperature coefficient and leakage current.
27	VCO	7		PLL adjustment-free VCO pin. Externally connect a Murata CSB912JF103 ceramic resonator.
28	PD2	7		Pilot detector pin of the FM stereo decoder block. Externally connect a capacitor of at least 0.22μF between this pin and V_{CC}. The capacitor should have a low temperature coefficient and leakage current. Pulling up this pin to V_{CC} disables the pilot cancel and VCO, and sets the outputs, including pin 32 (stereo mode output), to mono mode.

Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
29	SD	0		Outputs DC from the station detector. Externally connect a 100kΩ pull-up resistor between this pin and V_{DD}. The polarity of the pin is active high.
30	PNRin	3.6		Inputs the FM composite signal obtained from the FM decoder. Connect a capacitor between this pin and pin 31. Note that low capacitance reduces the low-frequency full separation.
31	Compo.	5		Outputs the audio signal decoded from the FM IF signal. Externally connect a capacitor between this pin and GND to eliminate carrier and other signals unnecessary for the next stage.
32	Mode-out			Stereo/mono FM receive mode output pin. Externally connect 2.2kΩ≦R≦22kΩ between this pin and the V_{DD}. In stereo mode, around 0.6V is generated. In mono mode, a V_{DD}-level output signal is generated. In stereo mode, connecting this pin to GND forcibly sets mono mode. However, pilot cancel, and the VCO in the 19kHz PLL still function.

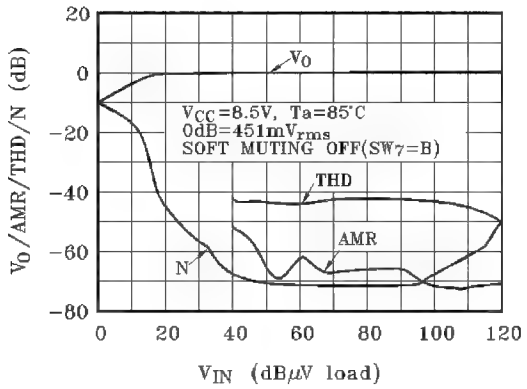
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
33	IFC	2.6		IF count output pin. This pin should be pulled up by a 3.3kΩ external resistor to 5V V_{DD}. In seek mode, set by the request pin, a 109dBμV (Typ.) IF counter signal is output to this pin. When not used, leave this pin open or connect to V_{DD}.
34	Request			Request pin. This pin is connected to the microcomputer. Pulling up to 3.3V (Typ.) or higher sets normal reception mode. Pulling down below 3.3V (Typ.) sets seek mode. In seek mode, station detection speed-up is enabled.
35	⊿F	5		⊿F detector output smoothing pin. Externally connect a capacitor. The time constant at requests should be shortened and station detection speeded up.

Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
36	Quad.	5		IF limiter amp output pin. Use a Toko 9067 as the external coil. Set FV conversion gain (FM decoder output) by the external R_D between pins 36 and 37. However, note that the SD bandwidth (135kHz Typ.) and the total harmonic distortion (THD) both change. The role of external capacitor 2 is to match the f_0 center with the lowest point of THD. Connect a capacitor of around 1pF. Check the capacitance, as the capacitance changes as a result of stray capacitance on the printed circuit board. The grounding point should be the IF reference or the IF-system GND. Adjust fo using the detector coil so that the potential difference between the IF reference and the ⊿F detector is "0". If the deviation is within ±30mV, the setting is within ±3kHz of 10.7MHz.
38	IFA2	5		

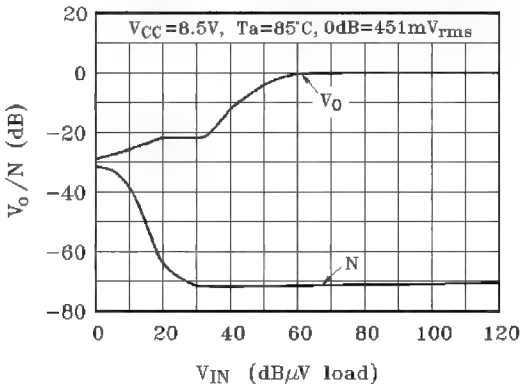
Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
37	Reg.	5		IF block reference voltage pin. Externally connect C≧0.047μF and RNC≧10kΩ. The RNC is used for setting the noise convergence for soft muting characteristics. The higher RNC1/RNC2 is set, the lower the noise convergence becomes. This pin also sets the amount of detuning muting, which is proportional to the noise convergence setting. Increasing the soft muting also increases the detuning muting. In general applications, RNC1 and RNC2 can be fixed resistors because an optimal meter output is obtained using pin 5 (Slide trimmer). The external front end gain deviation can also be absorbed by this output.
43	Muting	0		Sets the limiter sensitivity and the time constant for the soft muting. Externally connect a capacitor and R_M. The higher the R_M the higher the limiter sensitivity. Set the time constant using the capacitance value. As a general guide, the time constant should be around 1 ms.

Pin No.	PIN Name	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT/ EXTERNAL PARTS TYP. VALUE (INTERNAL R AND C VALUES ARE TYP. VALUES)	PIN FUNCTION
39	IFA2in	2.2		Input pin for IF limiter amp 2. Externally connect a ceramic filter.
40	IFA2 Bias	2.2		Bias pin for IF limiter amp 2. Ground this pin via a capacitor.
41	IFA1out	2.7		Output pin for IF limiter amp 1. Externally connect a ceramic filter.
42	GND	0		IF block GND pin.
44	V_{CC}	8.5		IF block V_{CC} pin.

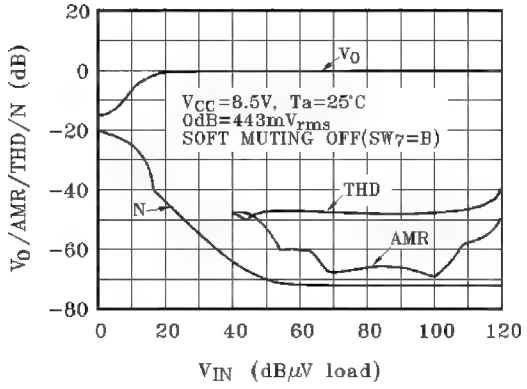
V_O /AMR/THD/N – V_{IN}



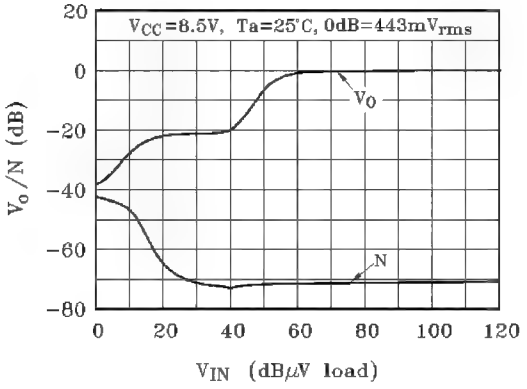
V_O /N – V_{IN} (SOFT MUTING)



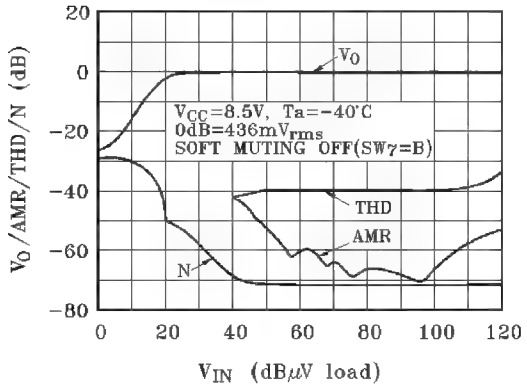
V_O /AMR/THD/N – V_{IN}



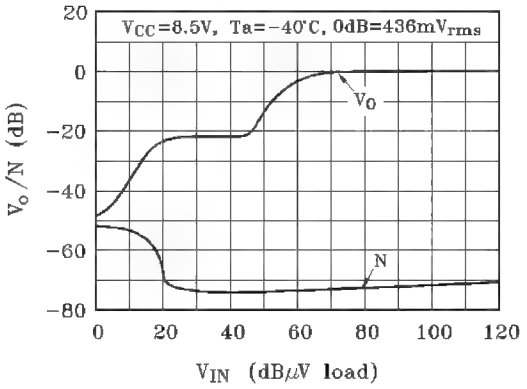
V_O /N – V_{IN} (SOFT MUTING)



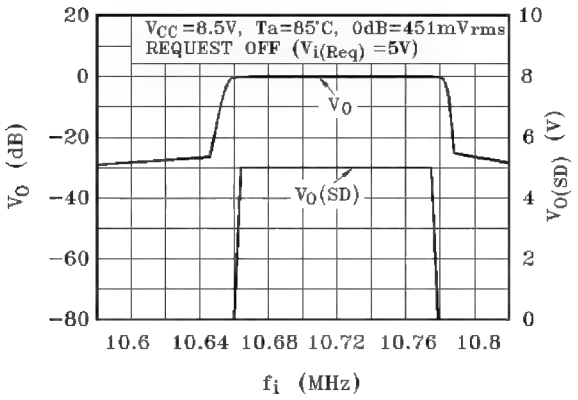
V_O /AMR/THD/N – V_{IN}



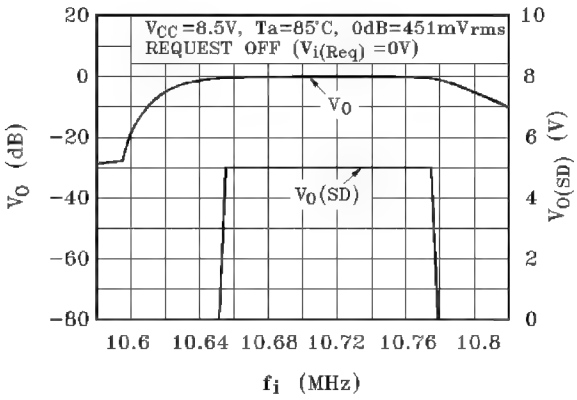
V_O /N – V_{IN} (SOFT MUTING)



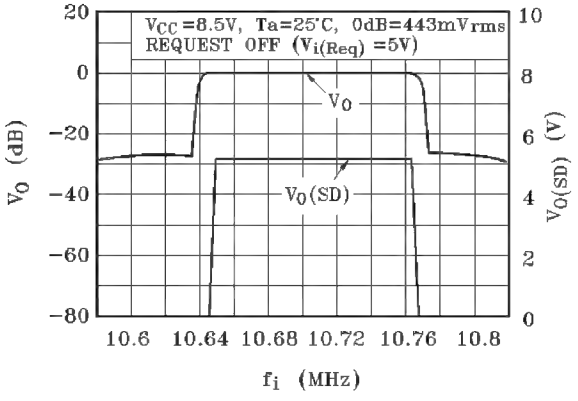
$V_O / V_O(SD)$ – f_i



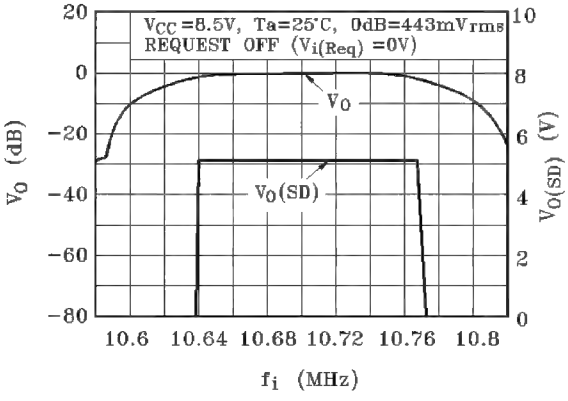
$V_O / V_O(SD)$ – f_i



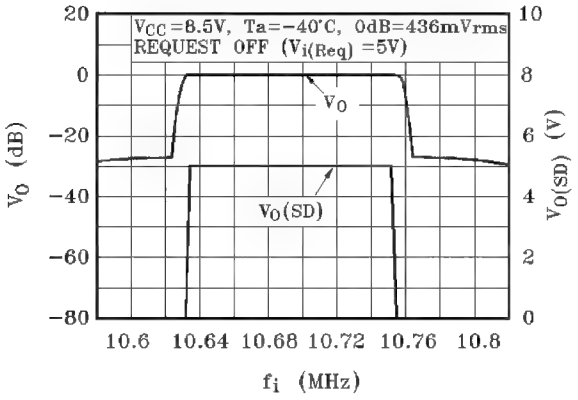
$V_O / V_O(SD)$ – f_i



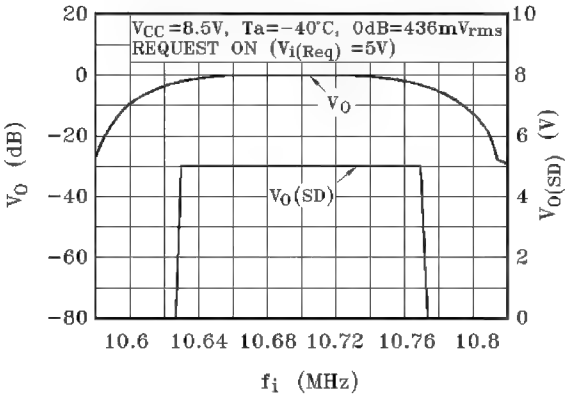
$V_O / V_O(SD)$ – f_i



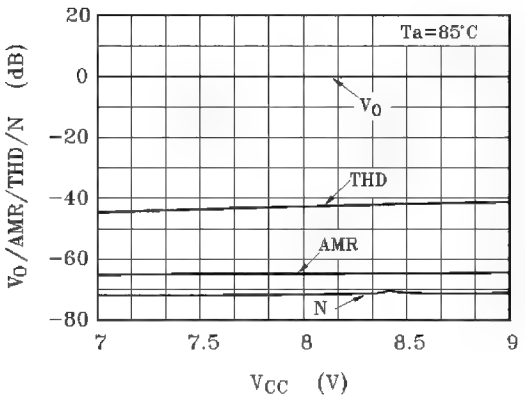
$V_O / V_O(SD)$ – f_i



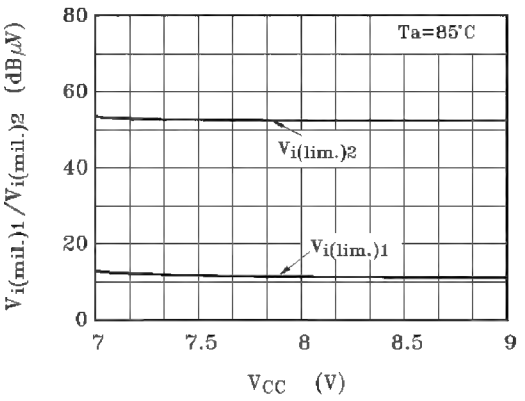
$V_O / V_O(SD)$ – f_i



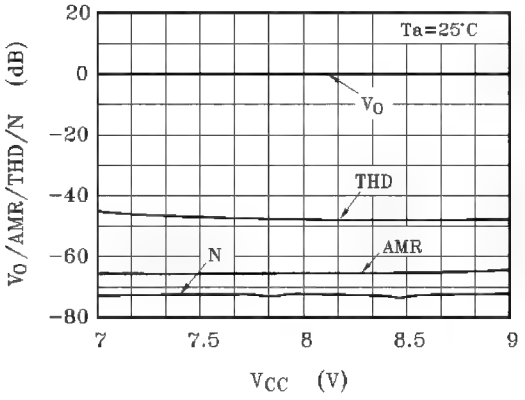
V_O /AMR/THD/N – V_{CC}



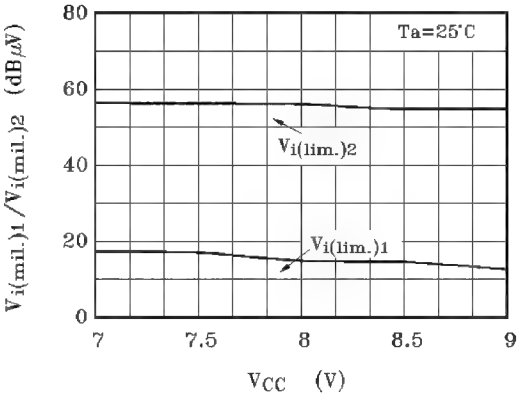
$V_{i(lim.)1}$ /$V_{i(lim.)2}$ – V_{CC}



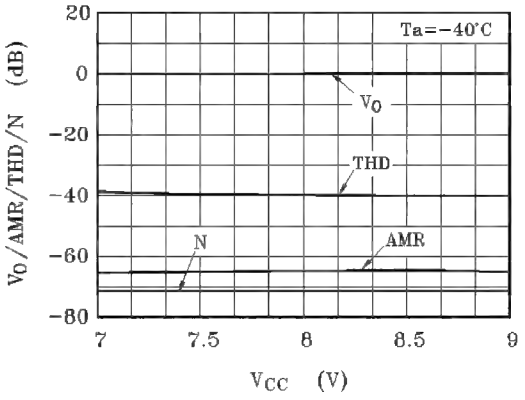
V_O /AMR/THD/N – V_{CC}



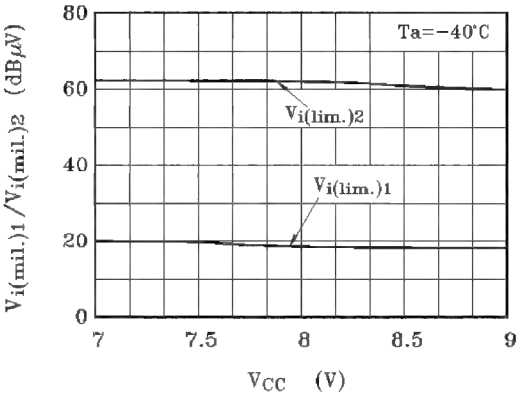
V_O /AMR/THD/N – V_{CC}



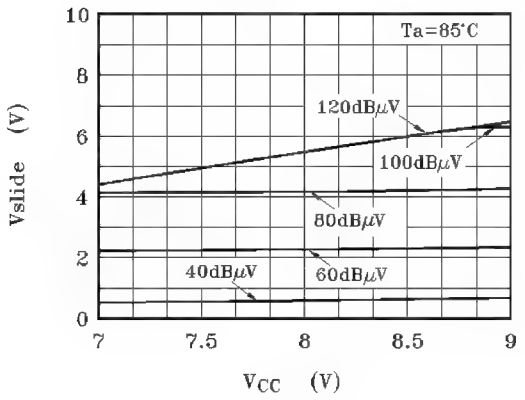
V_O /AMR/THD/N – V_{CC}



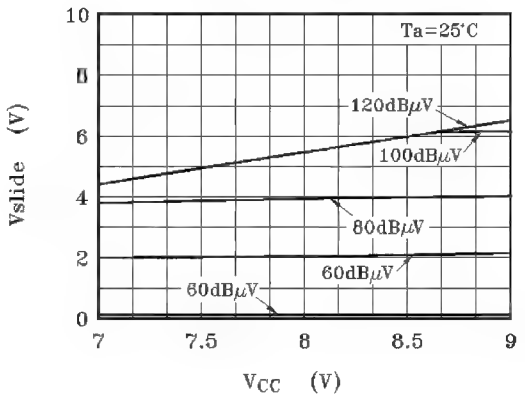
V_O /AMR/THD/N – V_{CC}



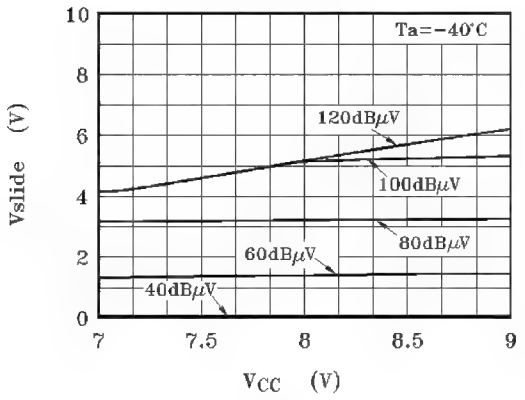
Vslide – V_{CC}



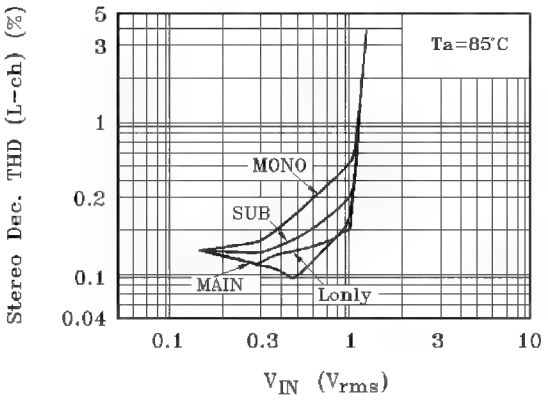
Vslide – V_{CC}



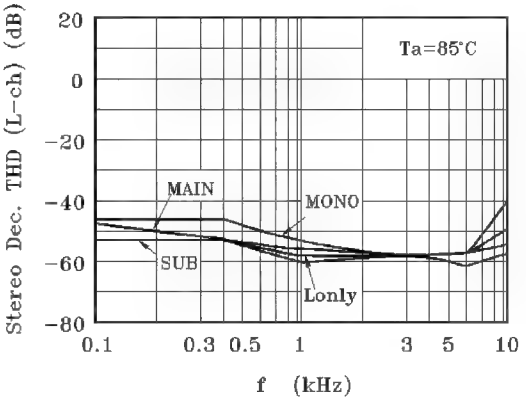
Vslide – V_{CC}



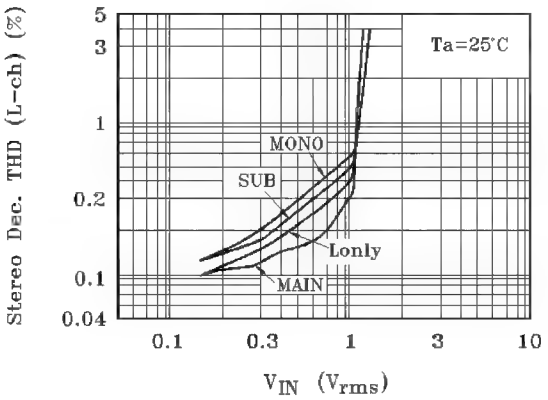
Stereo Dec. THD – V_{IN} (L-ch)



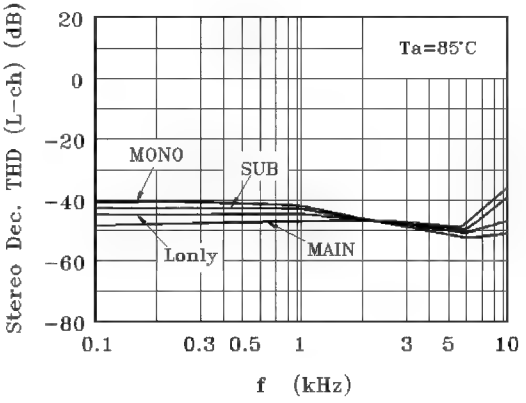
Stereo Dec. THD – f (L-ch)



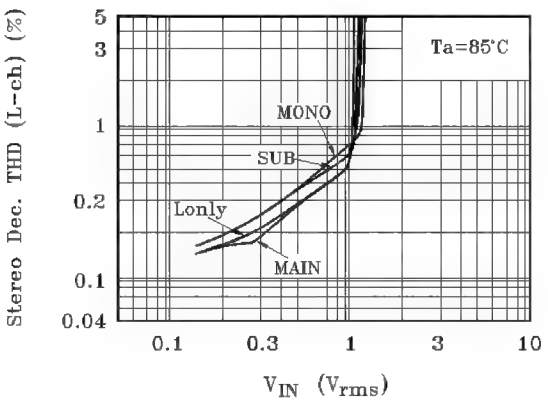
Stereo Dec. THD – V_{IN} (L-ch)



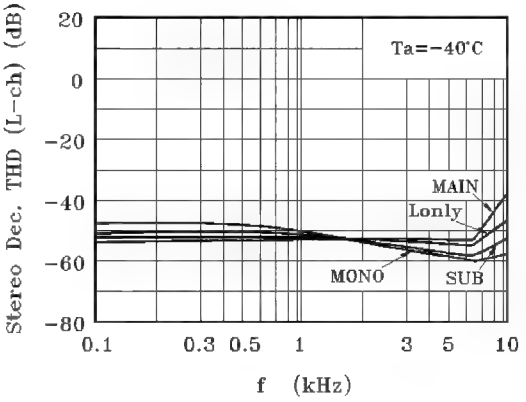
Stereo Dec. THD – f (L-ch)



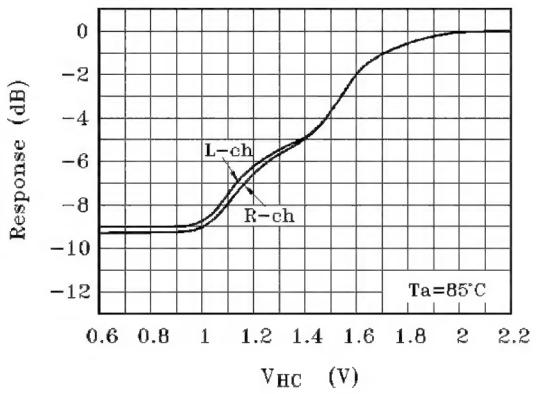
Stereo Dec. THD – V_{IN} (L-ch)



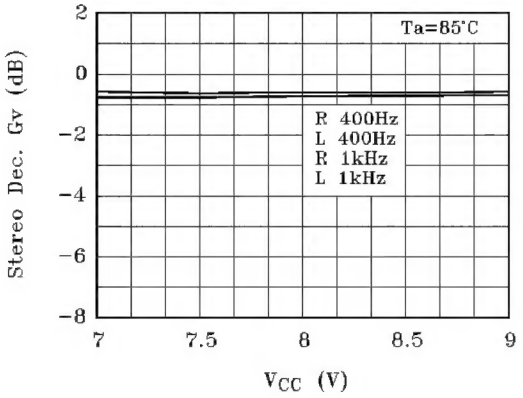
Stereo Dec. THD – f (L-ch)



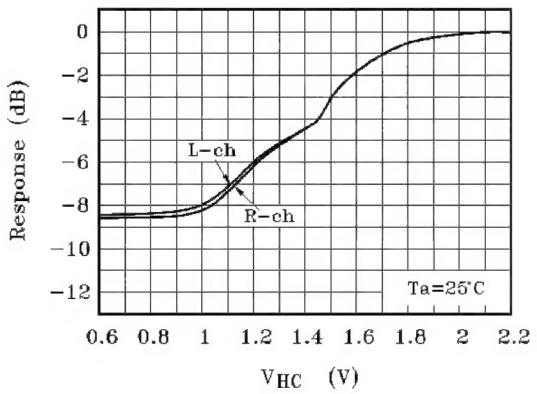
Signal(f=10kHz) – V_{HC}



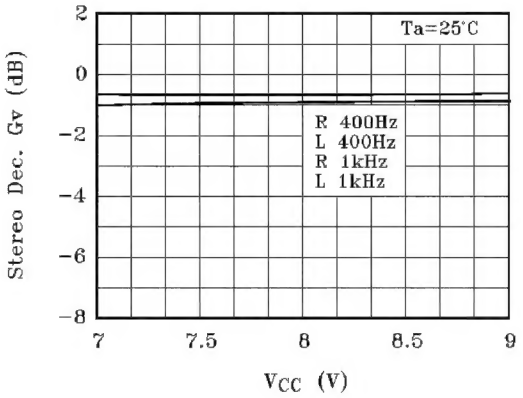
Stereo Dec. Gv – V_{CC}



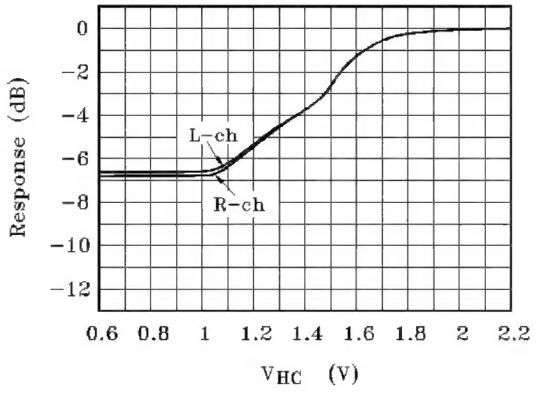
Signal(f=10kHz) – V_{HC}



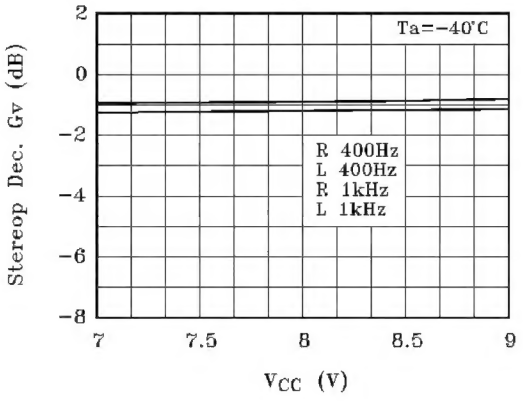
Stereo Dec. Gv – V_{CC}



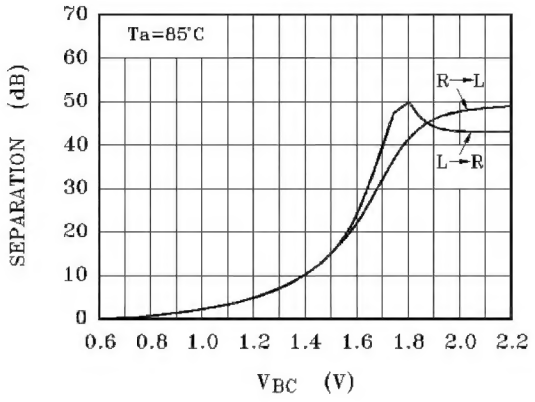
Signal(f=10kHz) – V_{HC}



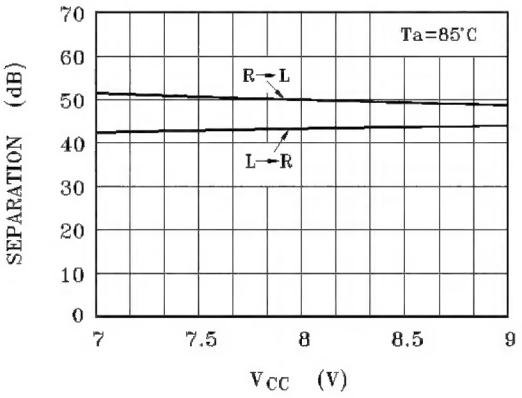
Stereo Dec. Gv – V_{CC}



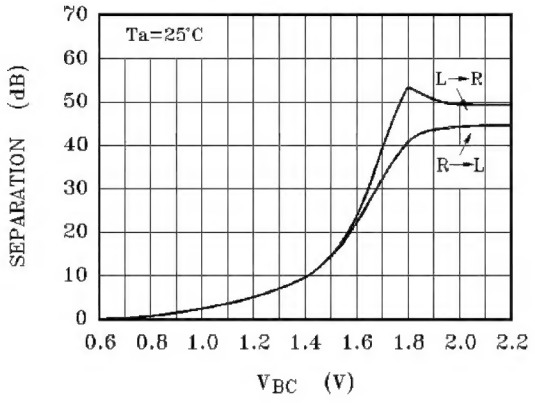
SEPARATION – V_{BC}



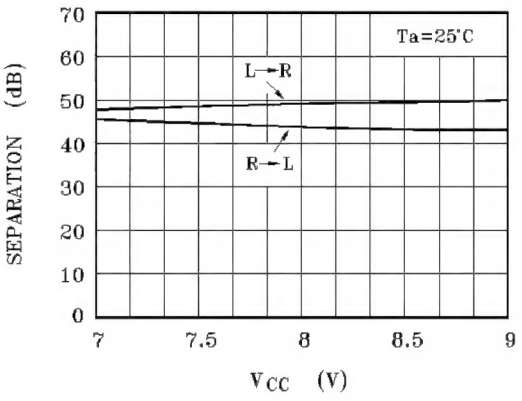
SEPARATION – V_{CC}



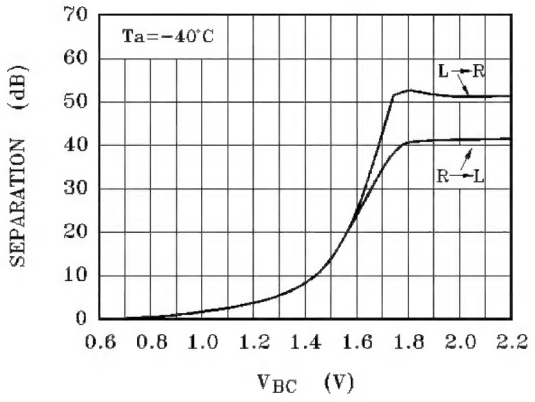
SEPARATION – V_{BC}



SEPARATION – V_{CC}



SEPARATION – V_{BC}



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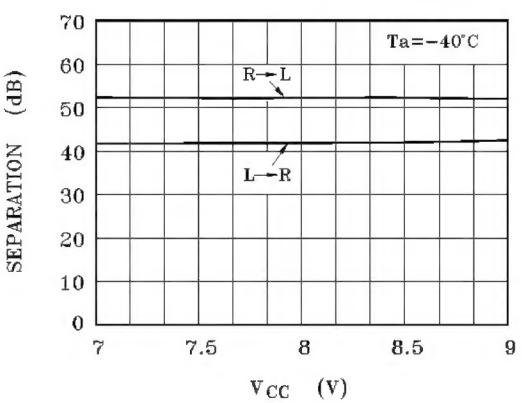
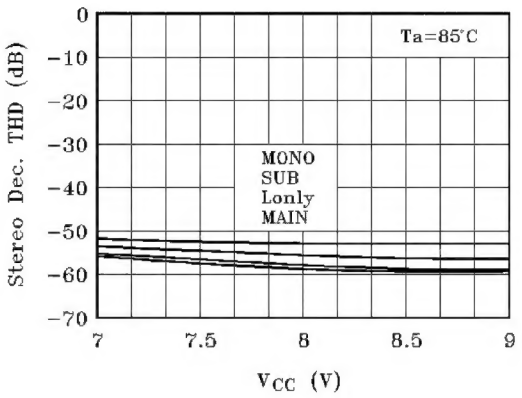
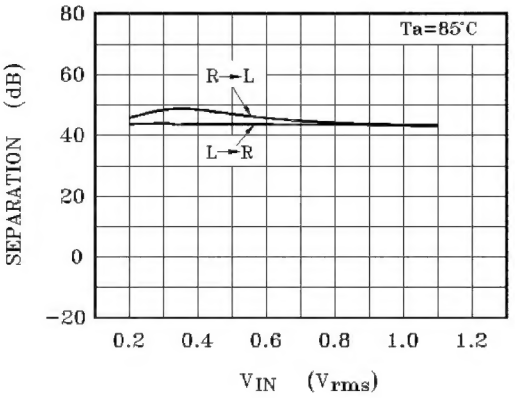


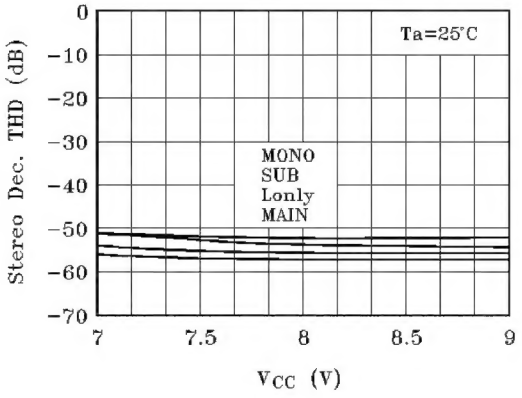
Stereo Dec. THD – V_{CC} (L-ch)



SEPARATION – V_{IN}



Stereo Dec. THD – V_{CC} (L-ch)



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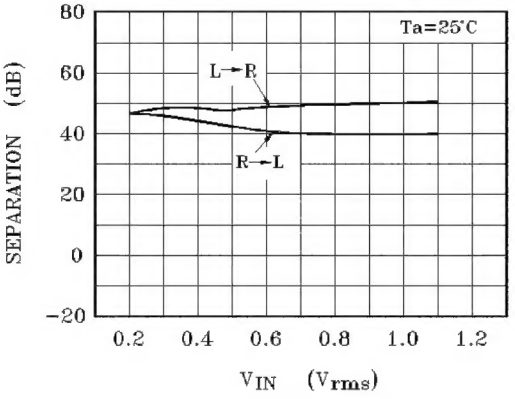
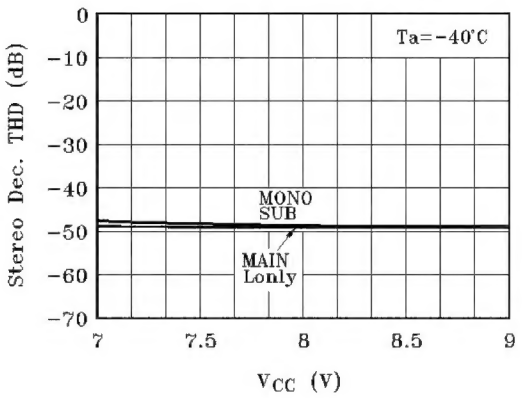


Stereo Dec. THD – V_{CC} (L-ch)



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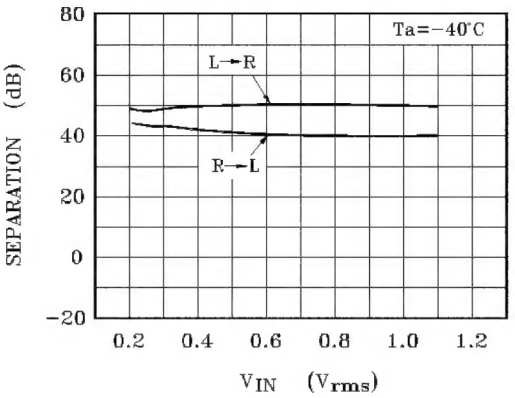

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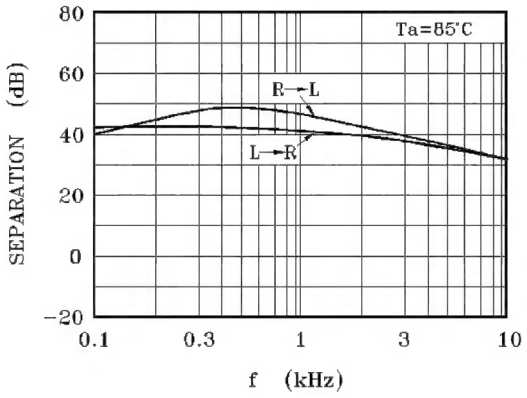

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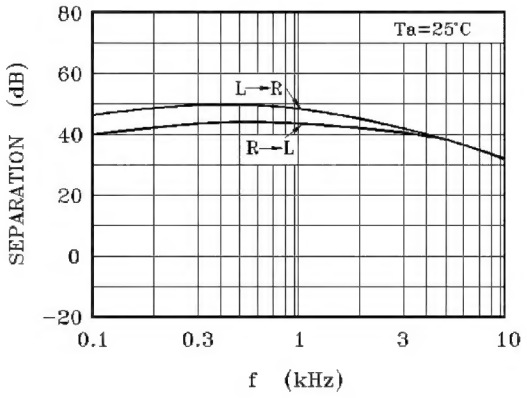

SEPARATION – f